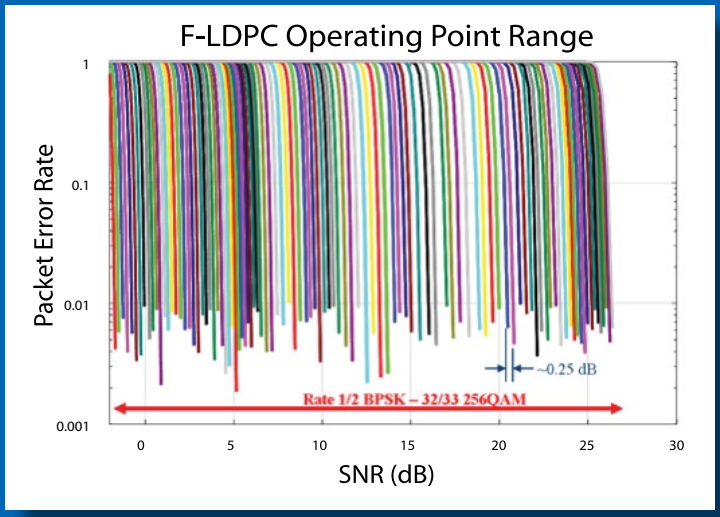
F-LDPC Product Family

Encoder and decoder cores

TrellisWare designed the Flexible Low-Density-Parity-Check (F-LDPC) codes to meet the demand in modern communication and storage systems for a highly flexible FEC solution that achieves very high data throughputs without compromising performance. These codes offer near capacity threshold performance and low error floors at low complexity. These properties make the F-LDPC the ideal forward error correction choice for many applications.

The F-LDPC is available as encoder and decoder cores for FPGA/ASIC implementations. The inherent flexibility of the F-LDPC means that the cores are highly configurable. Standard cores support 8 block sizes, 40 code rates, and 4 modulation types. Through Log Likelihood Ratio inputs the F-LDPC cores also support virtually any digital modulation type.



The figure above shows how the same F-LDPC decoder can support any operating SNR by choosing the code rate and the modulation type.

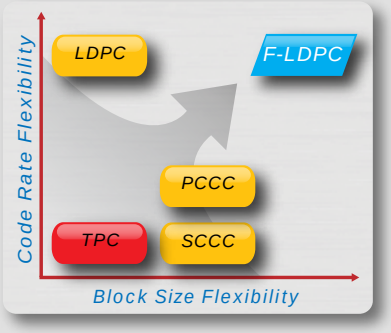
In addition, the F-LDPC cores are highly customizable. Custom block sizes can be quickly added to the product as requested before or after delivery via programmable ROM updates.

TrellisWare uses its patented decoding architectures to achieve throughputs in excess of 1 Gbps in FPGAs. ASIC implementations can result in much higher throughputs. TrellisWare's published data throughputs do not assume compromised threshold or floor performance.

TrellisWare® TECHNOLOGIES

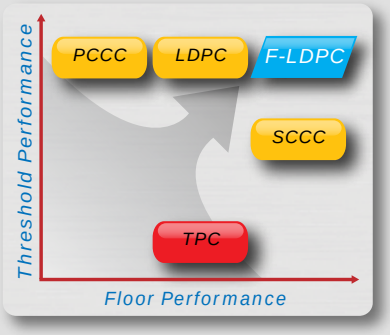
Key Features

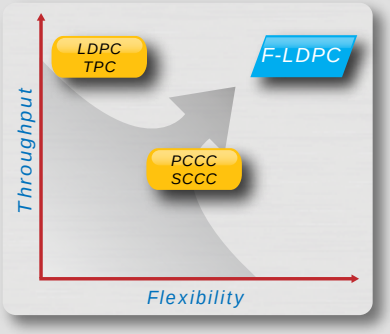
- Highly flexible and configurable in terms of block size, code rate and modulation types
  - Same decoder core supports any combination
  - Block sizes, code rates and modulation types can be changed on a block by block basis during operation
- Excellent performance
  - Near capacity threshold performance in all modes
  - Excellent floor/flare performance
- Highly customizable
  - Custom block sizes and code rates are added readily to standard decoders
- Very high data throughputs
  - > 1Gbps in FPGAs
  - ASIC implementations can result in much higher throughput
- Low complexity
  - Complexity for a given throughput or flexibility can be shown to be lower than other advanced FEC technologies



Single core supports multiple code rates and block sizes

Excellent threshold and error floor performance





Higher throughput and greater flexibility at low complexity

Part #	Data Throughput (Mbps) and Clock for FPGA	Minimum Target FPGA	Code Rates	Block Sizes
TW FP-100	6.25 @ 200 MHz	Altera EP2C8 Xilinx XC3S200	Each core supports 40 code rates from 1/2→32/33 8 standard block sizes: 128 bits→16K bits Programmable for virtually any other block size	
TW FP-200	50 @ 200 MHz	Altera EP2S30 Xilinx XC4LX25		
TW FP-300	90 @ 180 MHz	Altera EP2S60 Xilinx XC4LX40		
TW FP-400	180 @ 180 MHz	Altera EP2S60 Xilinx XC4LX60		
TW FP-500	333 @ 167 MHz	Altera EP2S130 Xilinx XC4LX100		
TW IFP-300	30 @ 150 MHz	Altera EP2S60 Xilinx XC4LX60	1/4, 1/3, 1/2	2K, 4K, 8K, 16K
Evaluation Software as C-library or Matlab DLL available for each core				

Applications

The unparalleled flexibility, the excellent threshold and floor/flare performance, the low complexity and the very high data throughputs of F-LDPC encoder and decoder cores are appealing to many customers with diverse applications - both in the government and commercial sectors. F-LDPC's flexibility allows many customers to choose the code in their early project/product development stages before they finalize their designs. TrellisWare offers ample support to these customers by providing software models for the encoder and decoder cores before the customer makes a decision, and offering the customer systems analysis expertise on issues ranging from modulation types to bit-widths. To date, we have had customers from a variety of applications from many sectors including:

- Satellite communications
- Robust military communications
- Commercial terrestrial wireless communications
- Magnetic and holographic storage systems
- Microwave point-to-point links
- Wireline communications
- 1.25 Gbps and above E-band point-to-point applications

Availability

TrellisWare has a proven track record of successfully integrating F-LDPC encoder/decoder cores into the products of a diverse customer base - both government and commercial. The FPGA/ASIC cores are available for immediate integration into customer systems.

About TrellisWare Technologies

TrellisWare Technologies, Inc. is a privately-held communications IP and products company headquartered in San Diego. Self funded since its incorporation in April 2000, TrellisWare has built a reputation as a leader in advanced communication algorithms, waveforms and turnkey communication systems that work when nothing else does. TrellisWare has developed a wide range of highly-advanced Forward Error Correction (FEC) algorithms and software defined radio (SDR) waveforms used in many military and commercial communication products. With deep expertise in radio physical layer design, networking, efficient high speed decoding, algorithm development and RF integration, TrellisWare is also developing a unique family of communication products capable of operating in the harshest RF environments.

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TrellisWare® TECHNOLOGIES

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