

ON THE DESIGN AND HARDWARE DEMONSTRATION OF A ROBUST, HIGH-SPEED FREQUENCY-HOPPED RADIO FOR SEVERE BATTLEFIELD CHANNELS¹

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ABSTRACT

The paper describes a robust, high-speed, frequency-hopping digital communication system that was designed, tested and implemented in hardware. Extensive trade-off analysis and simulations were performed for selecting the coding and modulation schemes, as well the receiver algorithms, that can achieve “turbo” -like performance. The implemented receiver combines Soft-Input/Soft-Output (SISO) equalization and decoding via Adaptive Iterative Detection (AID) techniques and exhibits excellent performance even in severe dynamic multipath fading channels with large delay spreads. Reduced complexity algorithms were also designed for hardware implementation and their performance was evaluated through numerical simulations and laboratory measurements. The system was successfully implemented in a hardware prototyping platform, and its performance in challenging dynamic fading channels was confirmed through laboratory demonstrations.

INTRODUCTION

This paper summarizes the development of a robust, high-speed, frequency-hopped, digital communication link suitable for mobile battlefield applications. This includes a description of the physical layer design (including modulation, coding, and receiver processing), the implementation of a board-level prototype, and the successful laboratory demonstration of the hardware prototype.

The motivation for this development, sponsored by the Army Research Labs (ARL), is provided by trends in battlefield requirements for data transmission. These trends include multi-user communication, moving platforms (e.g., ground vehicles or UAVs), severe propagation channels resulting from cluttered environments, and decentralized network control. As a result, the system design must cope with severe, time-

varying, frequency-selective fading and like-signal interference (e.g., co-channel interference (CCI)), while maintaining robustness to variations in these modeled channel impairments.

The communication link designed has the following characteristics:

- Robust and efficient digital communication at high rates,
- Excellent performance in challenging environments, enabling operation in severe multipath at carrier frequencies above 5 GHz with significant platform dynamics,
- Constant envelope modulation to permit efficient power amplification,
- Turbo-like coding performance,
- Frequency hopping for added robustness.

The resulting link can achieve throughputs of up to 512 kbps over channels with Doppler spreads of more than 500 Hz and delay spreads of up to 10 microseconds. The spectral efficiency, including training overhead, is approximately 1 bps/Hz on a per-hop basis. Even in this severe, frequency-selective Rayleigh fading channel, the performance of the link is comparable to that of a conventional, convolutionally encoded, AWGN channel.

In the course of this design effort, various encoding and modulation schemes were investigated to address these requirements. In concert with these investigations, receiver performance vs. complexity trades were optimized. Effective equalization of the severe fading intersymbol interference (ISI) channel was a primary challenge associated with the frequency hopped (FH) link design. With regard to this challenge, several advanced adaptive algorithms were considered:

- Equalization via Maximum Likelihood Sequence Detection (MLSD) techniques, such as Per Survivor Processing (PSP) and Conventional Adaptive MLSD (based on decision feedback channel estimation),

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- Combined equalization and decoding via Adaptive Iterative Detection (AID) techniques.

Reduced complexity techniques were explored in depth for the above family of algorithms. The best combination of performance, robustness, and hardware complexity was obtained using a reduced complexity Adaptive Iterative Detection algorithm based on a combination of approaches recently developed in academic research. Numerical simulations showed that a substantial performance improvement over traditional approaches is achieved. In addition, the design accommodates multiple antennas, special CCI mitigation processing, and support for some of the unique challenges of ad-hoc networking.

A fixed-point analysis of the entire system was performed, leading to the prototype implementation of the receiver in an FPGA/DSP-based generic signal-processing platform. Thus, the design is completely programmable and supports software defined radio architectures such as JTRS. Extensive lab testing using this prototype was conducted, validating the simulated performance in severe RF environments, including multipath fading and high Doppler spread.

CHALLENGES ASSOCIATED WITH HIGH DATA RATE, ROBUST MOBILE COMMUNICATIONS

When making a comparison of air-interface methods for such demanding environments, it is difficult to draw absolute conclusions. Each technique has some advantages and disadvantages. These are summarized below for some commonly suggested approaches:

OFDM: The primary strengths of OFDM are the ability to convert severe time delay spread from multipath into simple frequency domain processing due to frequency sub-channelization. This also allows for some degree of frequency agility, and OFDM techniques typically offer good spectral efficiency. A difficulty with OFDM is Large Peak-to-Average power ratio (PAR), requiring expensive linear amplifiers. OFDM is also susceptible to loss of frequency sub-channel isolation in the face of severe Doppler spreads that result from high dynamics.

Multi-Code Direct Sequence: An advantage is that this format is relatively robust to large variations in delay spread and Doppler spread, owing from the ability to use RAKE processing, which is memoryless. A disadvantage of this approach is the possible loss of bandwidth efficiency due to non-orthogonal channelization (i.e., orthogonal synchronous channelization is typically destroyed by channel effects). MC-DS systems are also susceptible to near-far interference. Furthermore, MC-DS

systems also suffer from significant PARs that create issues with non-linear PAs.

FH-Single-Carrier: A primary strength of this approach is the ability to use constant envelope signaling. The frequency-hopping permits frequency agility (i.e., one may avoid jammed hop frequencies), and relatively good spectral efficiencies can be achieved in severe mobile environments. Such systems are also less susceptible to near-far effects, which makes them suitable for ad-hoc networks, where power control is not an option. The primary challenge with this approach is equalization of large delay spreads caused in an effort to achieve high data throughput. The equalization problem includes the difficulty of tracking channel dynamics while using an equalization processor with memory, and achieving good performance against all ISI channel shapes experienced through fading. The need to handle all channel shapes leads to maximum-likelihood non-linear approaches. However, the complexity of this grows exponentially with the normalized delay spread (delay spread divided by symbol rate).

OVERVIEW OF SIGNAL DESIGN AND RECEIVER ALGORITHMS

Various modulation, coding and interleaving schemes, as well as receiver architectures were considered. Extensive analysis was performed to determine which combination of the above would provide the best performance with reasonable levels of implementation complexity. It is important to note that the final selection was made based on optimization of the performance/complexity of the entire system rather than optimization of individual elements.

A. Modulation and Coding Trade-offs

The CPM family of modulations was considered for their constant envelope property, which would allow use of efficient Class C power amplifiers. GMSK with BT=0.3 was selected over other binary, quaternary and octal CPM modulations due to its bandwidth efficiency and small spectral regrowth when used with inexpensive amplifiers.

Some of the investigated coding schemes are:

- Traditional convolutional codes (CC) [1],
- Parallel-concatenated CC (PCCC) (“turbo codes”) [2],
- Serial-concatenated CC (SCCC) [3],
- Serial-concatenated CC and CPM [4].

After extensive analysis, the serial-concatenated CC and CPM combination was selected. It provides the ability to

realize excellent performance with reasonable implementation complexity. This arrangement can also achieve large interleaver gains (“turbo” effect) with very low complexity of the inner code. This allows the channel equalizer and the inner decoder to be combined, reducing the overall complexity [4].

B. Receiver Processing Trade-offs

Due to the high channel symbol rate (1 Msps) and highly dynamic terrestrial operational environment (high Doppler fading rates, long delay spreads), the most challenging task was the equalizer design. Linear/DFE type solutions were discarded since they exhibit large SNR losses in fading environments. The main focus was placed on Adaptive Soft-Input Soft-Output (SISO) equalizers that can achieve significant gains when used in an iterative fashion.

A detailed trade-off of various adaptive and reduced complexity SISOs suggested in the literature [4][5][6] was conducted. Implementation of an adaptive SISO that would fully model the channel delay spread of 8 symbol times would require 512 states, and this number would increase exponentially with the channel delay spread. Therefore, reduced-complexity implementations were investigated. An implementation with 64 states was selected, as the performance degradation with respect to the fully modeled receiver is minimal, and the implementation benefits substantial.

The outer decoder was implemented as a fixed SISO with 16 states. A large interleaver was desirable to allow large achievable gains, and an interleaver of size 7648 was implemented. Each burst (hop) consists of 239 information bits, a short preamble and postamble, and front and back tail bits.

HARDWARE PROTOTYPE

The FH prototype receiver was implemented on the TrellisWare Advanced Signal Processing Engine and Communications Testbed (ASPECT), shown in Figure 1. The ASPECT board is a general-purpose computing platform ideally suited for communications-related signal processing, and contains four FPGAs, two DSPs, two DACs, two ADCs, and on-board RAM.

The processing blocks (SISOs, interleavers, etc) were written in VHDL and synthesized for the four FPGAs. One of the DSPs was used for configuring and controlling the hardware. The receiver was partitioned among the four FPGAs as shown in Figure 2. The input signal is received at an IF of 61.25 MHz and sampled at a rate of 35 MHz.

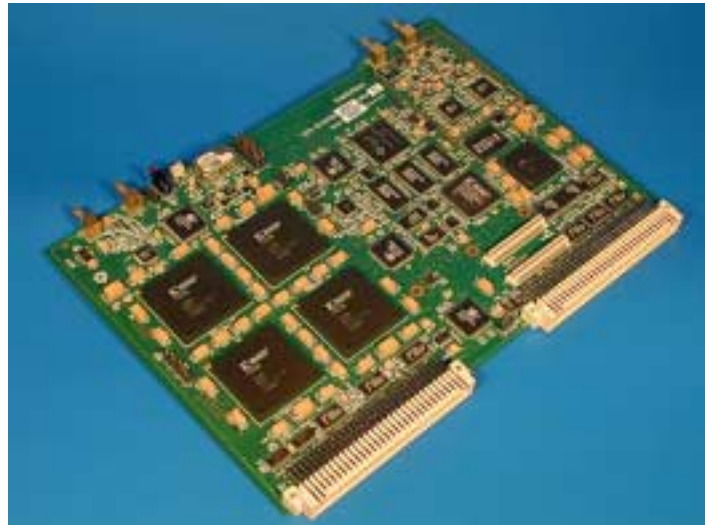


Figure 1 TrellisWare ASPECT prototyping platform

FPGA #2 contains a digital quadrature mixer and a series of decimating filters. The received waveform is mixed down to baseband and output at 2 samples/symbol (2 MHz).

FPGA #1 contains the circuitry that performs burst detection and timing alignment. When a burst is detected, the training sequences are used to generate channel estimates. These estimates and burst samples are passed to a double-buffer for iterative decoding. This double-buffer provides the maximum time for iterative decoding: While one block of data (32 bursts) is being received, the previous block of data is iteratively decoded.

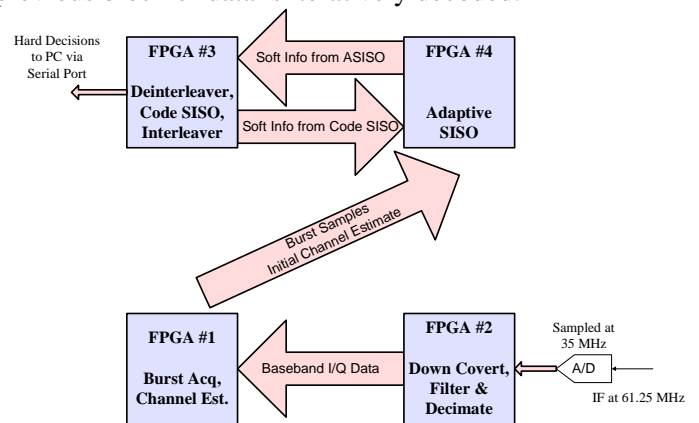


Figure 2 FPGA partitioning

FPGA #3 and FPGA #4 contain the two SISOs, the interleaver and the deinterleaver. A single iteration consists of a pass through the adaptive SISO, the deinterleaver, the code SISO, and the interleaver. Multiple iterations may be performed for improved performance. A hard decision is made on the output of the code SISO on the final iteration.

LABORATORY DEMONSTRATION

As mentioned previously, the ability to transmit successive bursts in different frequencies according to a predefined hopping pattern provides significant AJ capabilities. Another benefit of this FH receiver is that it can achieve significant gains in fading environments through iterative detection. In order to demonstrate this, a commercially available RF fading channel simulator was employed. Since this simulator has a rather narrow bandwidth compared to that of an FH signal, the bursts were spaced in time such that the fading processes observed in consecutive bursts would be uncorrelated. However, the FH receiver operates in real time at the burst symbol rate (1Msps).

A FH transmitter was also implemented on a second ASPECT board. This transmitter has the capability to accept input data through its serial port, or to generate pseudo-random data internally. This data is encoded, partitioned into bursts, and combined with training and tail sequences. The resulting signal is then modulated on a carrier of 1983 MHz and sent to the RF channel simulator. The output was downconverted to an IF of 61.25 MHz, added to calibrated noise, and fed to the ASPECT board that performs the receive functionality.

A video source was used as input data to the transmitter for demonstration. Since the data rate of the video signal was lower than the supported rate, the transmitted blocks were padded with PN data. The data output of the receiver

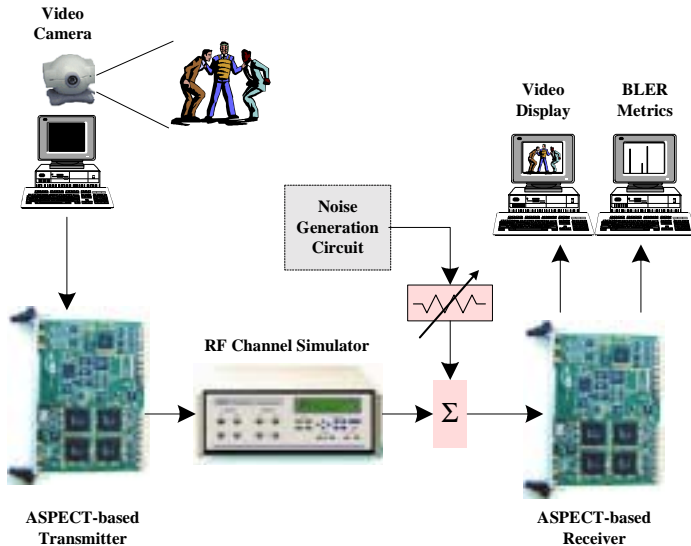


Figure 3 Block diagram of laboratory demonstration

was sent to two computers, one displaying the decoded video, the other computing error statistics in real time.

A block diagram of the lab demo is shown in Figure 3.

Selected performance results measured using the hardware laboratory testbed are presented in the following figures. Bit error rates in AWGN are shown in Figure 4 for each of the first 5 iterations. Measured results are compared with the expected performance obtained through numerical simulations. The lab results match simulation within the measurement tolerance of lab equipment (spectrum analyzer noise and power measurement capability).

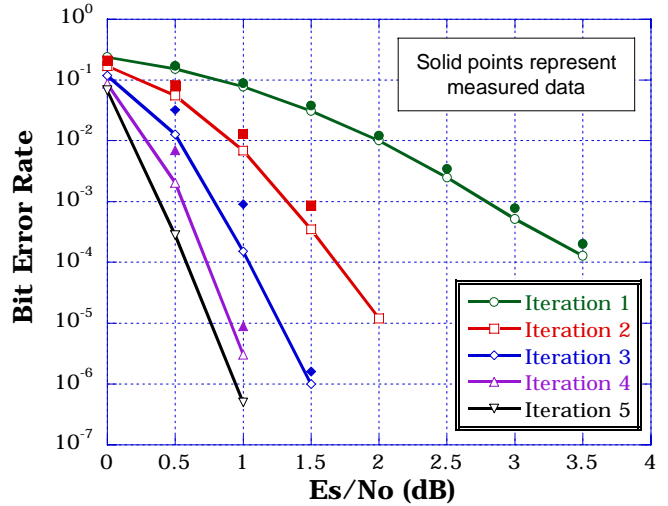


Figure 4 Simulated and measured BER in AWGN

Several multipath fading channel profiles were also investigated. Figure 5 shows measured block error rate in a typical urban environment [7] for a vehicle moving at 100 km/h.

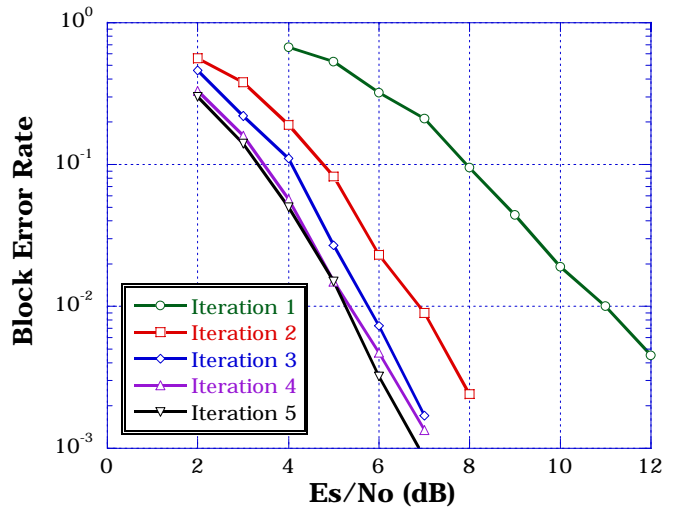


Figure 5 Measured BLER in a typical urban channel

Block error rate was also measured for an equalization channel with 10 Rayleigh fading taps of equal power and

spaced uniformly over a total delay spread of $9\mu\text{s}$; results are presented in Figure 6.

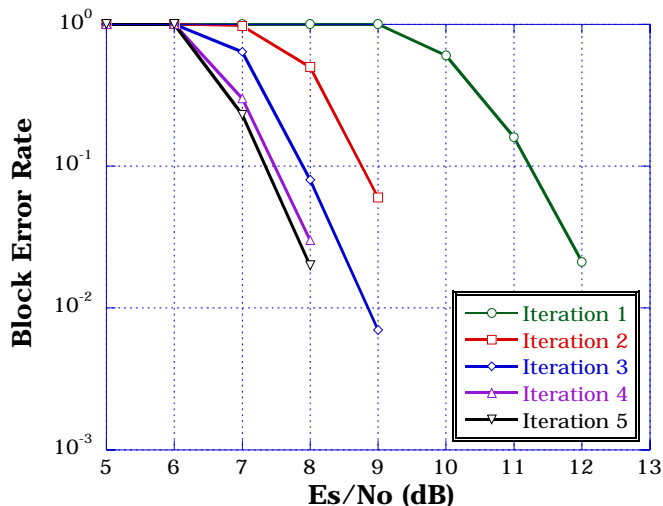


Figure 6 Measured BLER in an equalization channel

CONCLUSIONS

This paper described the design and implementation of a robust, high-speed, frequency-hopping, mobile digital communication link suitable for various battlefield applications. The physical layer analysis and design trades resulted in selection of coding and modulation schemes, as well as receiver architectures that provided significant performance improvement compared to conventional receivers. The implemented receiver algorithms employ combined SISO equalization and decoding through AID techniques that offer turbo-like performance through iteration. Hardware prototypes of the designed transmitter and receiver were successfully developed, showing that such architectures are realizable with current technology. Extensive numerical simulations and laboratory measurements were conducted which successfully validated the resulting hardware implementation.

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REFERENCES

- [1] G.C. Clark, and J.B. Cain, *Error-Correction Coding for Digital Communications*, New York, NY, Plenum Press, 1981.
- [2] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limit Error-Correcting Coding and Decoding: Turbo Codes," *Proc. 1993 IEEE Int. Conf. Comm.*, pp. 1064-1070.
- [3] S. Benedetto and G. Montorsi, "Serial concatenation of block and convolutional codes," *Electron. Lett.*, vol. 32, no. 10, pp. 887-888, May 1996.
- [4] K. Chung, K. M. Chugg, J. Heo, "Reduced State Adaptive SISO Algorithms for Serially Concatenated CPM over Frequency-selective Fading Channels," *Proc. Globecom 2001*, Nov. 2001, San Antonio, pp. 1162-1166.
- [5] K. M. Chugg, A. Anastasopoulos, and X. Chen, *Iterative Detection: Adaptivity, Complexity Reduction, and Applications*, Kluwer Academic Press, 2001.
- [6] P. Thiennviboon, G. Ferrari and K. M. Chugg, "Generalized Trellis-based Reduced-State Soft-Input/Soft-Output Algorithms," *ICC 2002*, New York, May 2002.
- [7] European Telecommunications Standard Institute (ETSI), Rec. ETSI/GSM 05.05.